CLAIMS

1. A method for forming, by epitaxy, a heteroatomic single-crystal semiconductor layer on a single-crystal semiconductor wafer, the crystal lattices of the layer and of the wafer being different, comprising forming, before the epitaxy, in the wafer surface, at least one ring of discontinuities around a useful region, said discontinuities being at least one rough area.

2. The method of claim 1, wherein the layer is a silicon-germanium layer and the wafer is a silicon trench.

3. The method of claim 1, wherein an insulating trench is formed, after the epitaxy, at the ring location, said trench surrounding an active area intended to contain at least one elementary component.

4. The method of claim 1, wherein said rings have a square or rectangular shape and their limits are arranged according to paths of subsequent cutting of the wafer in electronic chips.

5. The method of claim 1, wherein the roughness of said rough area exhibits a mean square deviation ranging between 10 and 30 nm.

6. The method of claim 1, wherein an additional single-crystal semiconductor layer is formed by epitaxy on the heteroatomic layer, the natural crystal lattice of the material forming the additional layer being different from that of the heteroatomic layer, whereby the additional layer is strained according to the lattice of the heteroatomic layer.

7. The method of claim 6, wherein the additional layer is a silicon layer.

8. A single-crystal semiconductor wafer covered with a heteroatomic single-crystal semiconductor layer, the crystal lattices of the layer and of the wafer being

different, wherein the wafer surface comprises at least one discontinuity ring around a useful region.

9. The wafer of claim 8, wherein the heteroatomic layer is a silicon-germanium layer and the wafer is a silicon wafer.